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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,103	12/17/2001	Michiaki Maruoka	NECB 19.265	3507
7590 03/09/2004 Katten Muchin Zavis Rosenman 575 Madison Avenue New York, NY 10022-2585			EXAMINER NGUYEN, KHIEM D	
			ART UNIT 2823	PAPER NUMBER
DATE MAILED: 03/09/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/024,103

Applicant(s)

MARUOKA, MICHIAKI

Examiner

Khiem D Nguyen

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 15-20 is/are rejected.
- 7) ☒ Claim(s) 11-14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Amendment*

The non-final rejection as set forth in paper No. (7) is withdrawn in response to applicants' amendments. A new rejection is made as set forth in this Office Action.

Claims (1-20) are pending in the application.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent 6,597,032) in view of the Applicant's Admitted Prior Art in this application (AAPA).

In re claim 1, Lee discloses a semiconductor device having a bonding pad electrode of a multi-layer structure, the semiconductor device comprising (col. 3, line 63 to col. 5, line 29 and **FIGS. 1-4e**): a semiconductor substrate (**FIG. 4d: 100**); a lower electrode layer (**FIG. 4d: 108 a and 108b**) formed on the semiconductor substrate; a cover insulating film (**FIG. 4d: 110 and 114**) formed on the lower electrode layer (col. 4, lines 26-39), wherein the cover insulating film has an opening (**FIG. 4d: h2 and h3**) for exposing at least a portion of the lower electrode layer (col. 4, lines 40-61), a step portion is provided at a side wall of the opening of the cover insulating film (**FIGS. 4d-e**), the size of the opening at the upside portion of a step surface of the step portion (opening at

layer **114**) is larger than the size of the opening at the downside portion of the step surface (opening at layer **110**); and an upper electrode layer (**FIG. 4d: 118a and 118b**) formed on the portion of the lower electrode layer exposed via the opening, and the upper electrode layer overlaps the step surface of step portion (col. 5, lines 3-29).

Lee does not explicitly disclose wherein the upper electrode layer being made of material having corrosion resistance against substance which is corrosive to the lower electrode layer.

AAPA discloses wherein the upper electrode layer (**FIGS. 14B-C: 103**) being made of material (TiNiAg) having corrosion resistance against substrate which is corrosive to the lower electrode layer (**FIGS. 14B-C: 101**) (Background of the Invention, pages 2, lines 2-16). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Lee and AAPA to enable the upper electrode layer having corrosion resistance of Lee to be formed and furthermore to obtain a bonding pad electrode structure in which the lower electrode **101** can be protected from a corrosive substance which can corrode aluminum (col. 2, lines 2-4).

In re claim 2, AAPA discloses wherein the cover insulating film comprises a silicon nitride film and a PSG (phospho silicate glass) film formed on the silicon nitride film, the step surface of the step portion being a surface portion of the silicon nitride film (Background of the Invention, pages 1 and 3).

In re claim 3, AAPA discloses wherein the cover insulating film (**FIG. 14A: 102**) comprises a PSG film (Background of the Invention, page 1, lines 25-26).

In re claim 4, AAPA discloses wherein the lower electrode layer (**FIG. 14B: 101**) comprises a metal film containing aluminum (Background of the Invention, page 2, lines 2-4), and the upper electrode layer (**FIG. 14B: 103**) comprises a metal film which has corrosion resistance against substance corrosive to aluminum (Background of the Invention, page 2, lines 6-16).

In re claim 5, AAPA discloses wherein the upper electrode layer (**FIG. 14B: 103**) comprises a TiNiAg film (Background of the Invention, page 2, lines 9-16).

In re claim 6, AAPA discloses wherein the device further comprising a high conductivity metal plate coupled onto the upper electrode layer via a conductive paste (Background of the Invention, page 1).

In re claim 7, AAPA discloses wherein the conductive paste is an Ag paste, and the metal plate is a copper plate (Background of the Invention, page 1).

In re claims 8 and 9, AAPA discloses wherein said bonding pad electrode is a source pad electrode of a power MOSFET (Background of the Invention, page 1, lines 18-24).

2. Claims 10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent 6,597,032) in view of the Applicant's Admitted Prior Art in this application (AAPA).

In re claim 10, Lee discloses a method of manufacturing a semiconductor device having a bonding pad electrode of a multi-layer structure, the method comprising (col. 3, line 63 to col. 5, line 29 and **FIGS. 1-4e**): preparing a semiconductor substrate (**FIG. 4d: 100**); forming a lower electrode layer (**FIG. 4d: 108 a and 108b**) on the semiconductor

substrate; forming a cover insulating film (**FIG. 4d: 110 and 114**) on the lower electrode layer (col. 4, lines 26-39), forming an opening (**FIG. 4d: h2 and h3**) in the cover insulating film to expose at least a portion of the lower electrode layer, wherein a step portion is provided at a side wall of the opening of the cover insulating film, the size of the opening at the upside portion of a step surface of the step portion (col. 4, lines 40-61 and **FIGS. 4d-e**), the size of the opening at the upside portion of a step surface of the step portion (opening at layer **114**) is larger than the size of the opening at the downside portion of the step surface (opening at layer **110**); and forming an upper electrode layer (**FIG. 4d: 118a and 118b**) on the portion of the lower electrode layer exposed via the opening, and the upper electrode layer overlaps the step surface of step portion (col. 5, lines 3-29).

Lee does not explicitly disclose wherein the upper electrode layer being made of material having corrosion resistance against substance which is corrosive to the lower electrode layer.

AAPA discloses wherein the upper electrode layer (**FIGS. 14B-C: 103**) being made of material (TiNiAg) having corrosion resistance against substrate which is corrosive to the lower electrode layer (**FIGS. 14B-C: 101**) (Background of the Invention, pages 2, lines 2-16). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Lee and AAPA to enable the upper electrode layer having corrosion resistance of Lee to be formed and furthermore to obtain a bonding pad electrode structure in which the lower electrode 101 can be protected from a corrosive substance which can corrode aluminum (col. 2, lines 2-4).

In re claim 15, AAPA discloses wherein the lower electrode layer (**FIG. 14B: 101**) comprises a metal film containing aluminum (Background of the Invention, page 2, lines 2-4), and the upper electrode layer (**FIG. 14B: 103**) comprises a metal film which has corrosion resistance against substance corrosive to aluminum (Background of the Invention, page 2, lines 6-16).

In re claim 16, AAPA discloses wherein the upper electrode layer (**FIG. 14B: 103**) comprises a TiNiAg film (Background of the Invention, page 2, lines 9-16).

In re claim 17, AAPA discloses wherein the device further comprising coupling a high conductivity metal plate onto the upper electrode layer via a conductive paste, after forming the upper electrode layer on a portion of the lower electrode layer exposed via the opening (Background of the Invention, page 1).

In re claim 18, AAPA discloses wherein the conductive paste is an Ag paste, and the metal plate is a copper plate (Background of the Invention, page 1).

In re claims 19 and 20, AAPA discloses wherein said bonding pad electrode is a source pad electrode of a power MOSFET (Background of the Invention, page 1, lines 18-24).

***Allowable Subject Matter***

Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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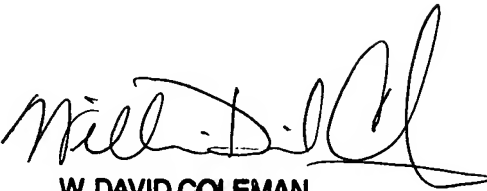
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.  
March 5, 2004

  
**W. DAVID COLEMAN**  
**PRIMARY EXAMINER**